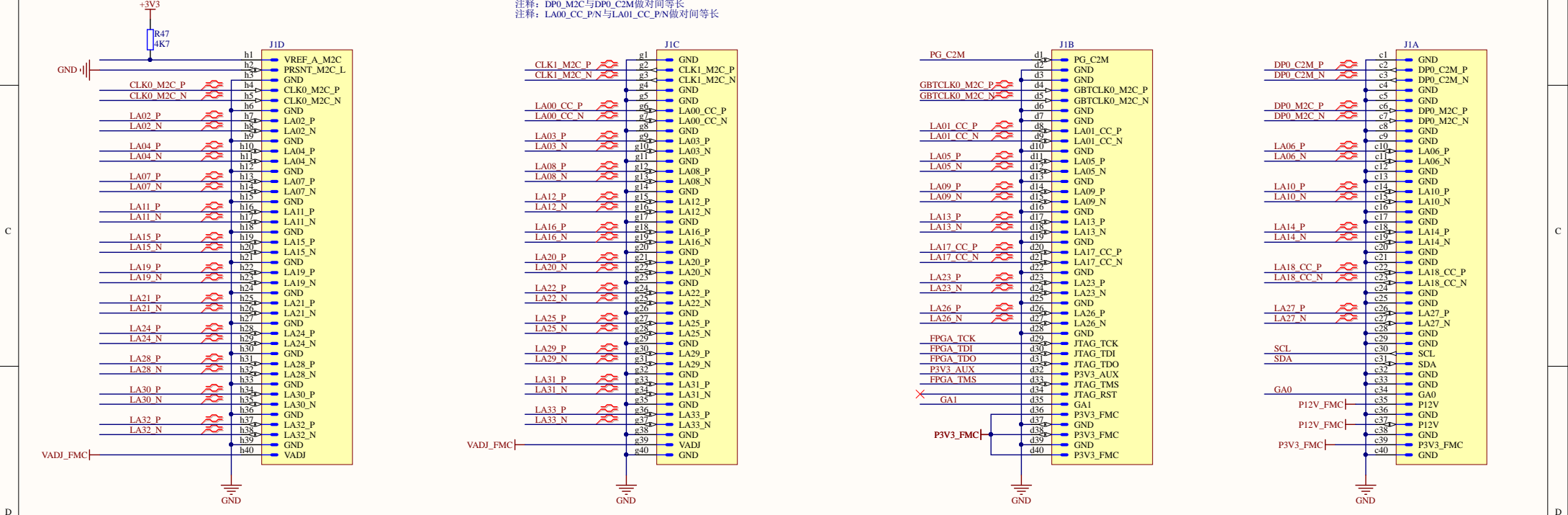
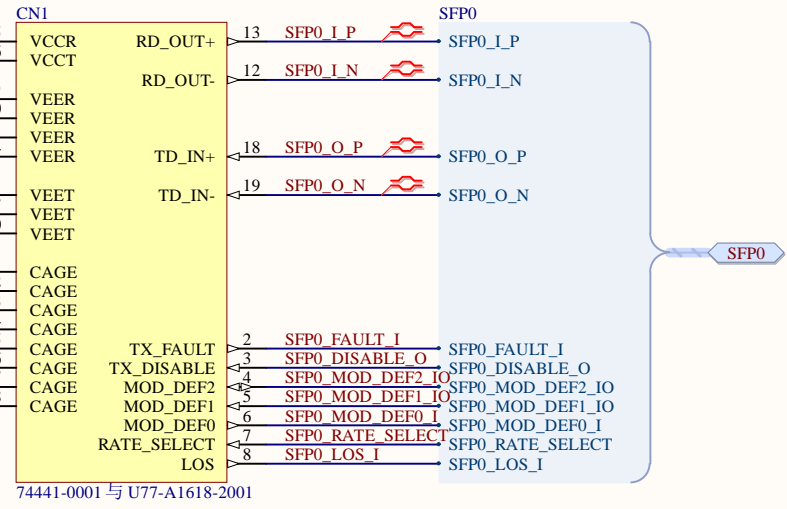
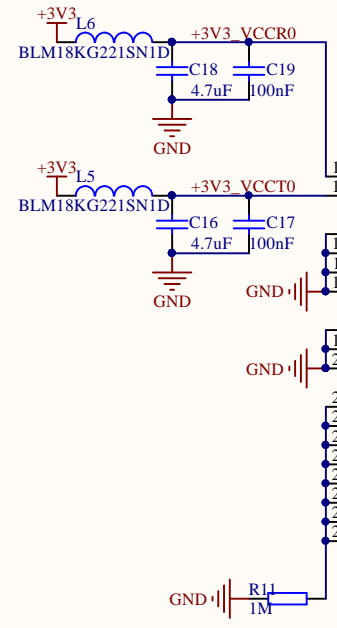
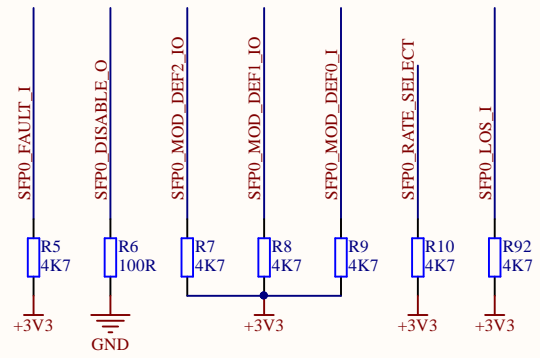


注释: LA_XX全部做对间等长
 注释: CLK0_M2C与CLK1_M2C做对间等长
 注释: DP0_M2C与DP0_C2M做对间等长
 注释: LA00_CC_P与LA01_CC_P做对间等长

注释: 差分信号DP0_C2M_P/N需要做对内等长, DP0_M2C_P/N需要做对内等长, 误差小于2mil
 注释: 差分信号DP0_C2M_P/N/DP0_M2C_P/N需要做对间等长, 误差小于2mil



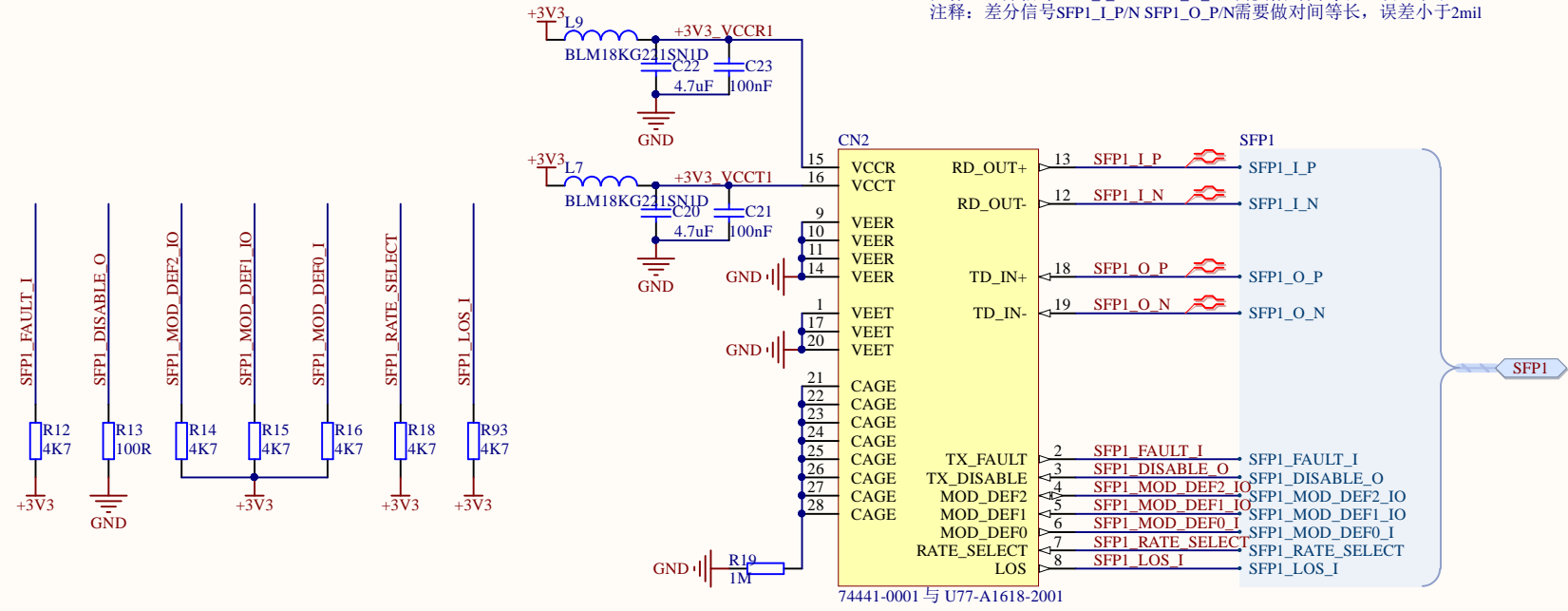
Title		
Size	Number	Revision
A3		
Date:	2022/8/19	Sheet of
File:	D:\WorkDir\1\CON_FMC.SchDoc	Drawn By:



注释：差分信号SFP0_I_P/N 需要做对内等长，SFP0_O_P/N需要做对内等长，误差小于2mil
 注释：差分信号SFP0_I_P/N SFP0_O_P/N需要做对间等长，误差小于2mil
 注释：差分信号SFP0_O_P/N SFP1_O_P/N需要做对间等长，误差小于2mil

Title		
Size	Number	Revision
A4		
Date:	2022/8/19	Sheet of
File:	D:\WorkDir\...\CON_SFP0.SchDoc	Drawn By:

注释：差分信号SFP1_I_P/N 需要做对内等长，SFP1_O_P/N需要做对内等长，误差小于2mil
 注释：差分信号SFP1_I_P/N SFP1_O_P/N需要做对间等长，误差小于2mil
 注释：差分信号SFP1_I_P/N SFP1_O_P/N需要做对间等长，误差小于2mil



74441-0001 与 U77-A1618-2001

Title		
Size	Number	Revision
A4		
Date:	2022/8/19	Sheet of
File:	D:\WorkDir\...\CON_SFP1.SchDoc	Drawn By:

1

2

3

4

A

A

B

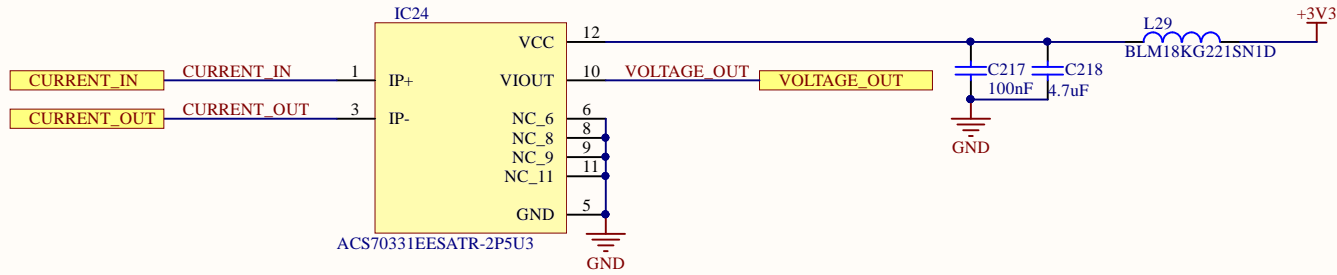
B

C

C

D

D



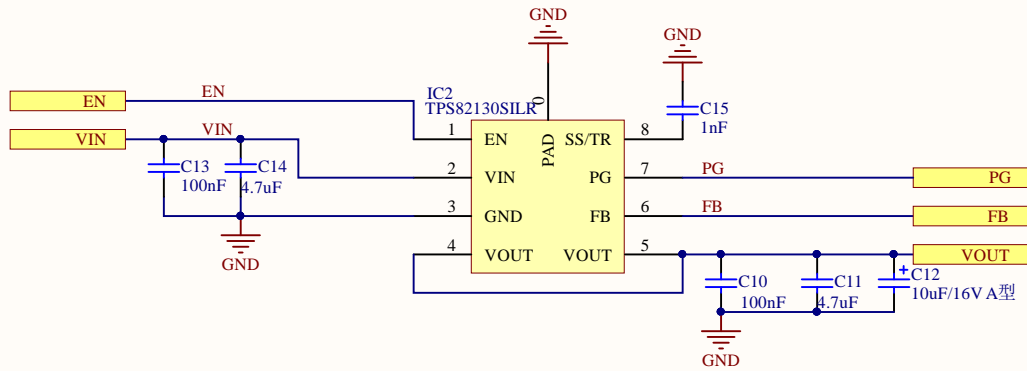
Title		
Size A4	Number	Revision
Date: 2022/8/19	Sheet of	
File: D:\WorkDir\..\CURRENT_SENSOR.Sch Drawn By:		

1

2

3

4

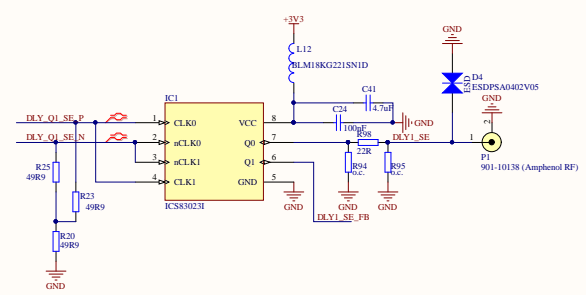
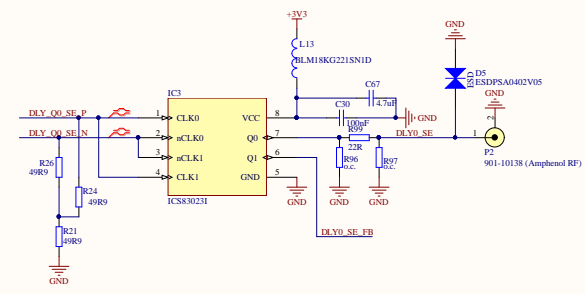
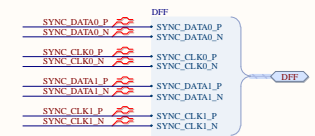
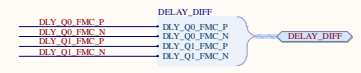
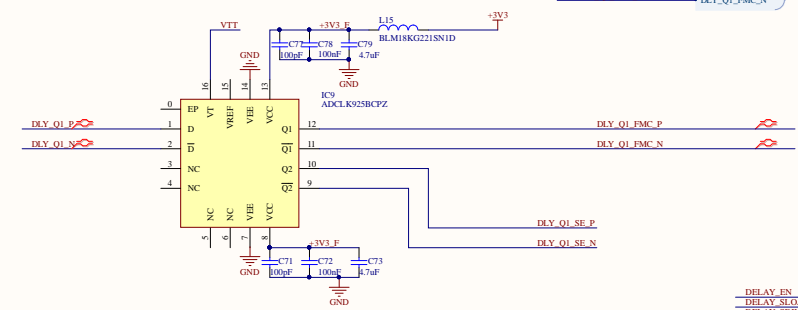
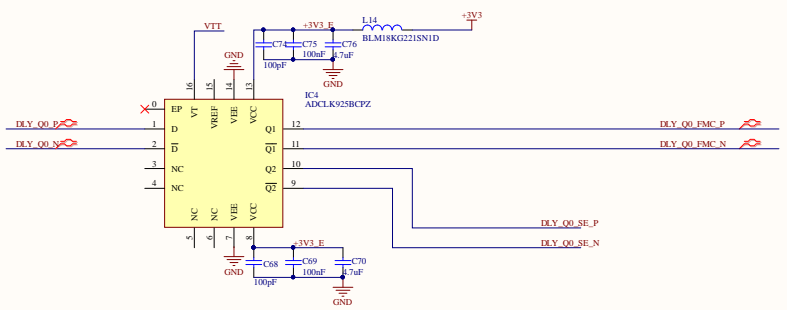
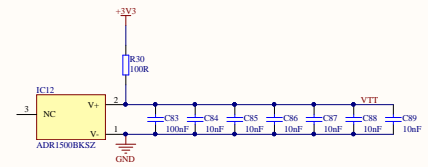
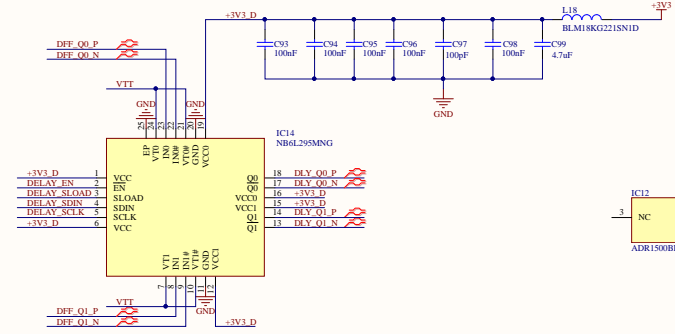
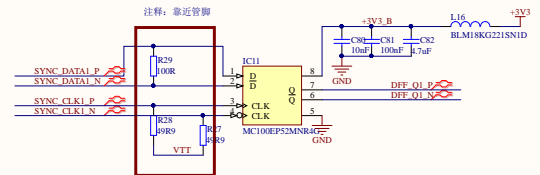
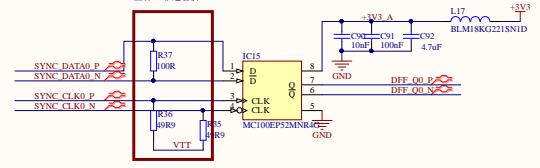


注释：电源线请加粗 不低于15mil

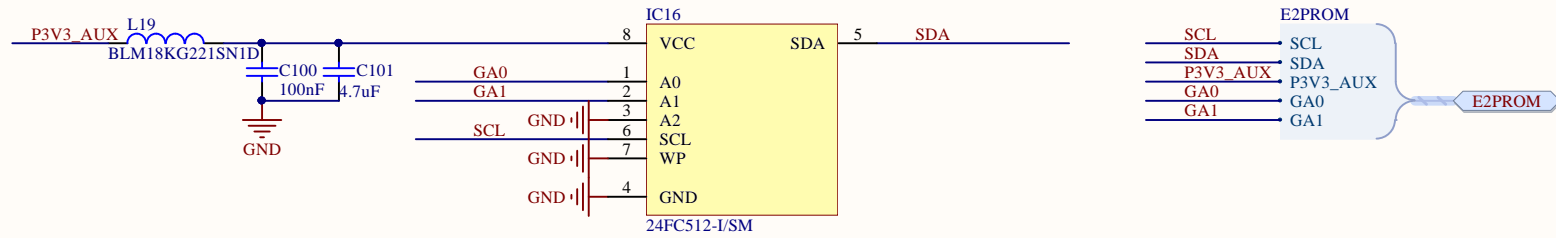
Title		
Size A4	Number	Revision
Date: 2022/8/19	Sheet of	
File: D:\WorkDir\..\DCDC_3A.SchDoc	Drawn By:	

注释：差分信号内部需要做对内等长，误差小于 2mil
 注释：此端尾端为 0 1 的差分对需要做对间等长，误差小于 2mil

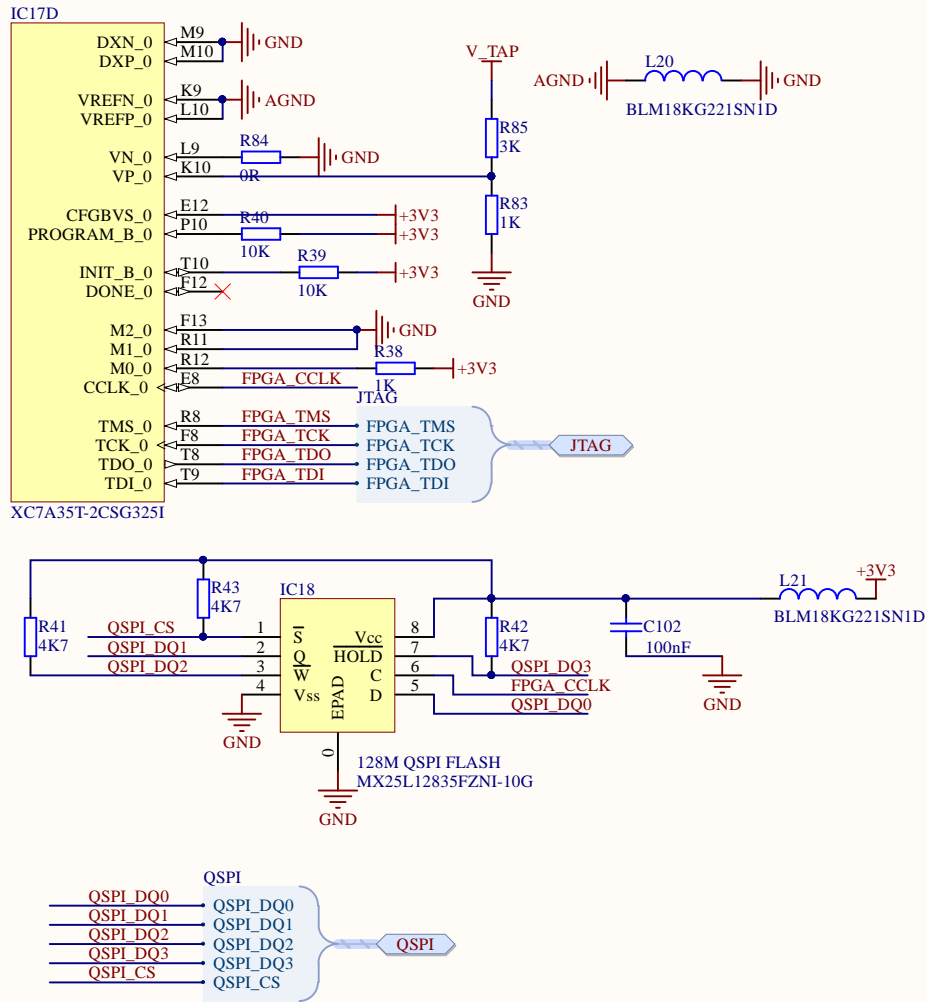
注释：靠近管脚



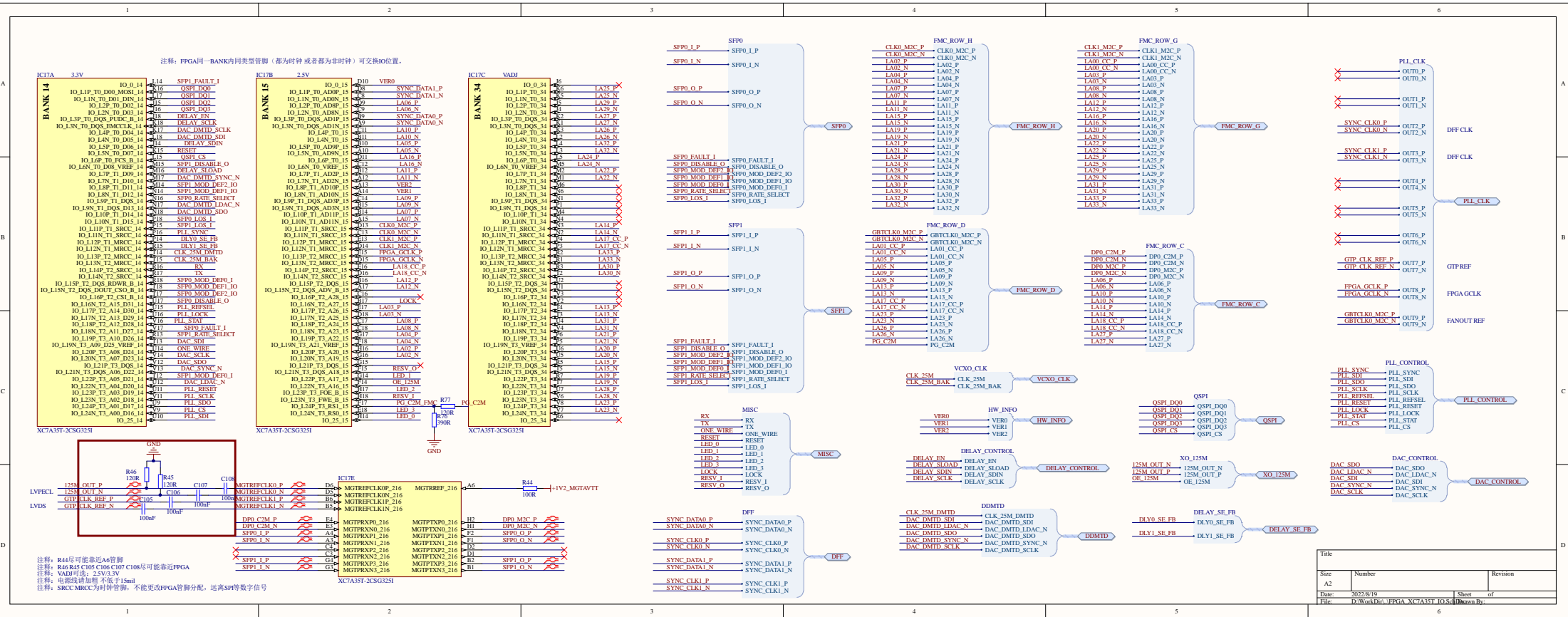
Title		
Size	Number	Revision
A2		
Date:	2023/8/19	Sheet 04
File:	D:\Work\2023\DFP_DELAY_FANOUT_Schematic.B...	



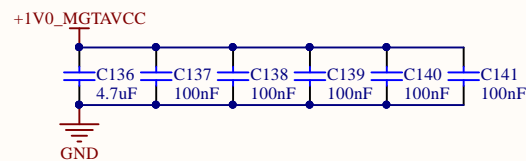
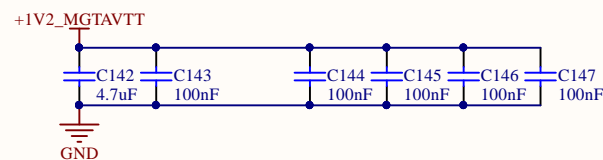
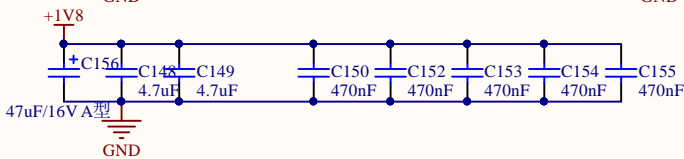
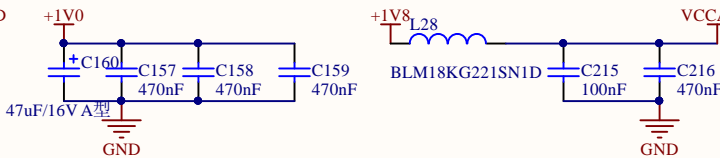
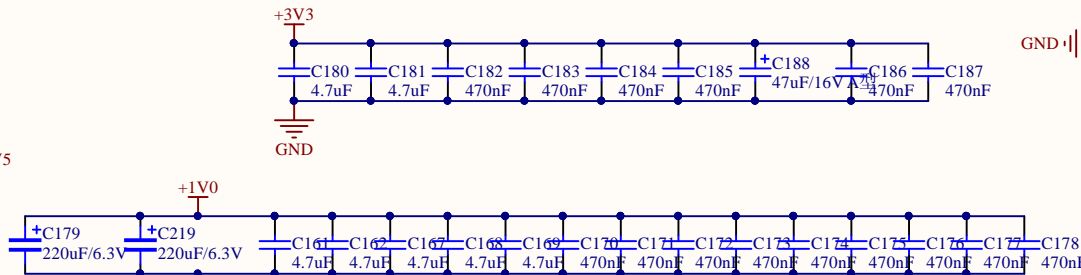
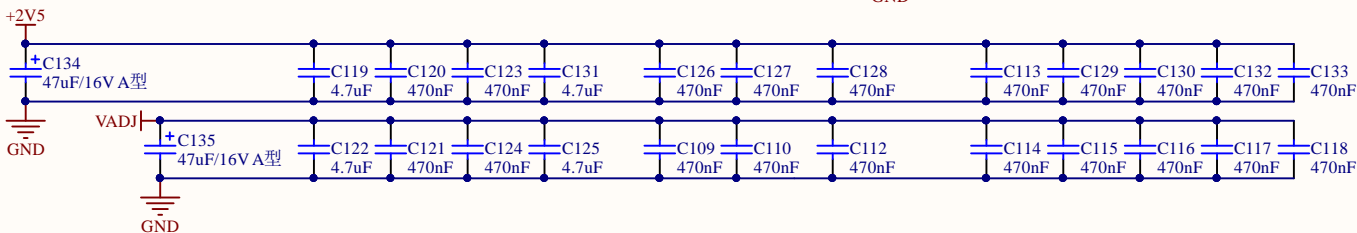
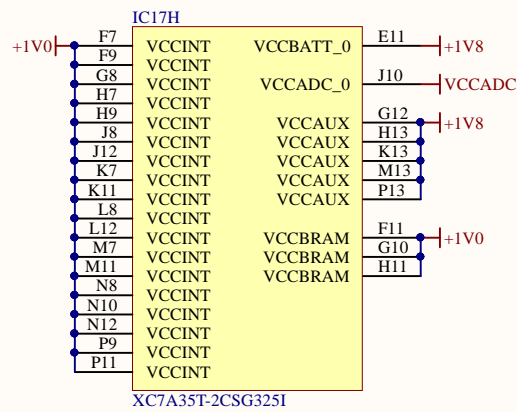
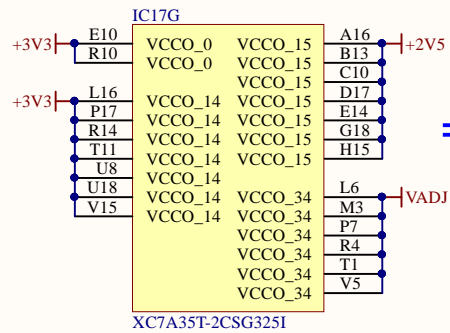
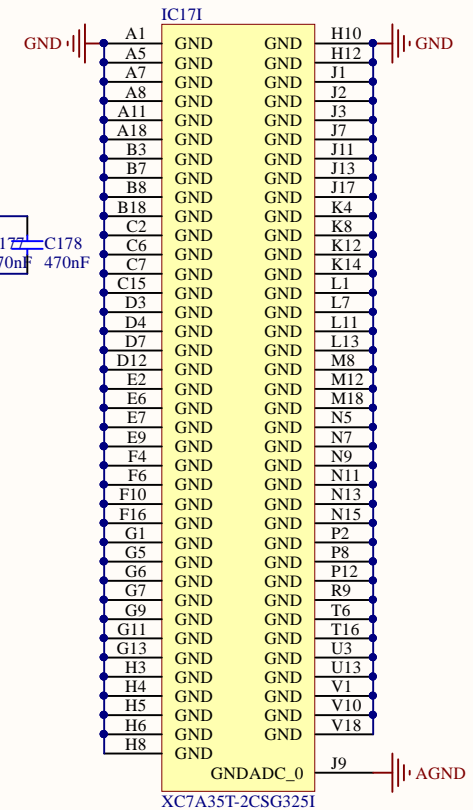
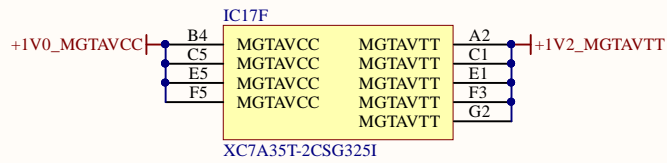
Title			
Size	Number		Revision
A4			
Date:	2022/8/19	Sheet	of
File:	D:\WorkDir\..\E2PROM.SchDoc	Drawn By:	



Title		
Size A4	Number	Revision
Date: 2022/8/19	Sheet of	
File: D:\WorkDir\...\FPGA_XC7A35T_CONF	Drawn by:	

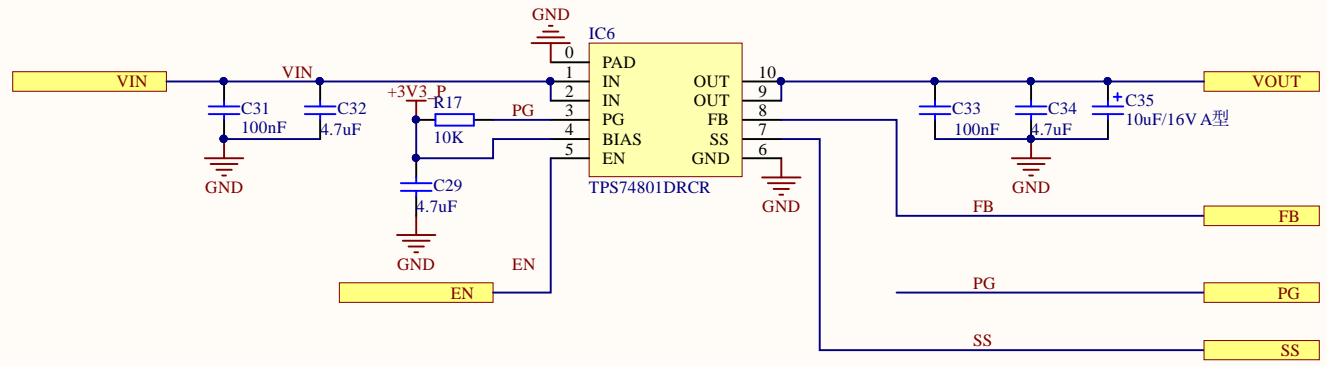


Title		
Size	Number	Revision
A2	30228/19	
Drawn		Sheet of
File:	D:\Work\06_FPGA_XC7A35T_IO_Sch	Drawn By:



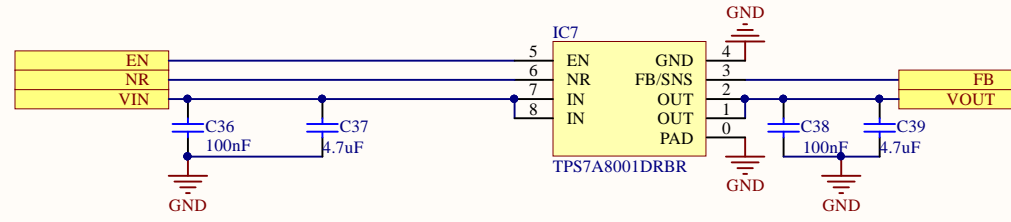
注释: 100nF电容尽量布局在焊盘旁边, 一对一放置
注释: 电源线请加粗 不低于15mil

Title		
Size	Number	Revision
A4		
Date:	2022/8/19	Sheet of
File:	D:\WorkDir\...\FPGA_XC7A35T_POWER_Schematic.dwg	



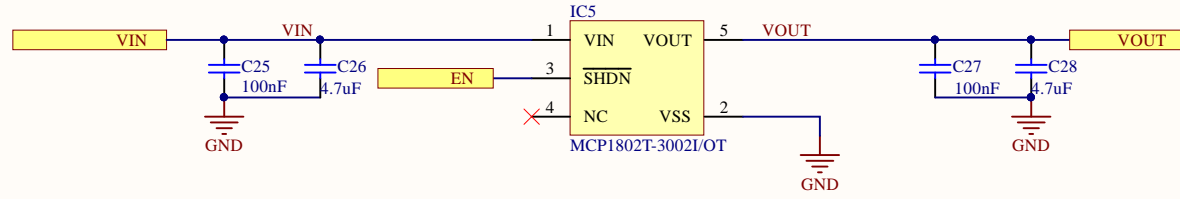
注释：电源线请加粗 不低于15mil

Title		
Size	Number	Revision
A4		
Date:	2022/8/19	Sheet of
File:	D:\WorkDir\...\LDO_GTP_1.5A.SchDoc	Drawn By:



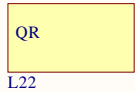
注释：电源线请加粗 不低于15mil

Title		
Size	Number	Revision
A4		
Date:	2022/8/19	Sheet of
File:	D:\WorkDir\..\LDO_IO_1A.SchDoc	Drawn By:



注释：电源线请加粗 不低于15mil

Title		
Size	Number	Revision
A4		
Date:	2022/8/19	Sheet of
File:	D:\WorkDir\...\LDO_XO_0.3A.SchDoc	Drawn By:



L22

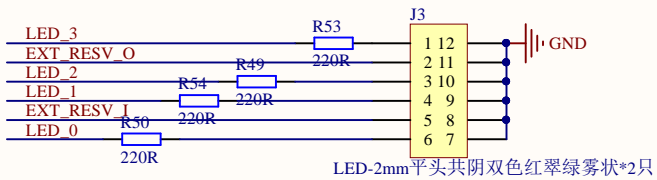
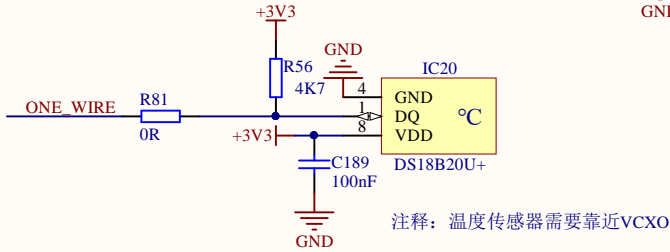
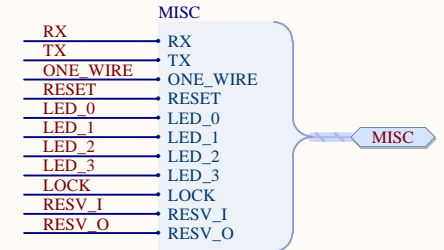
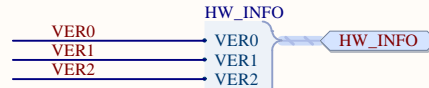
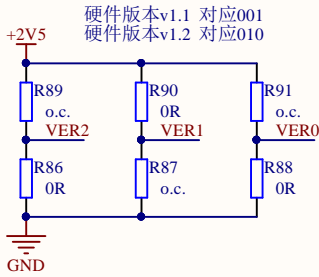


ESD_W1

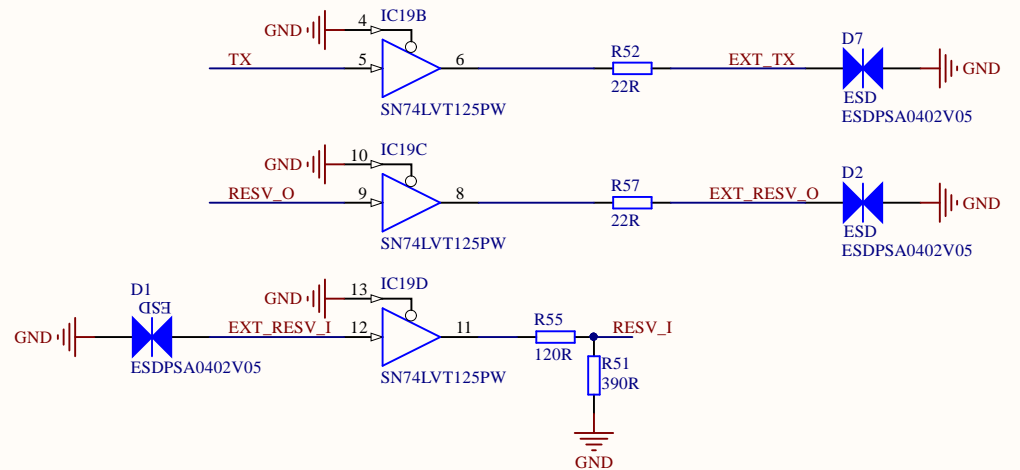
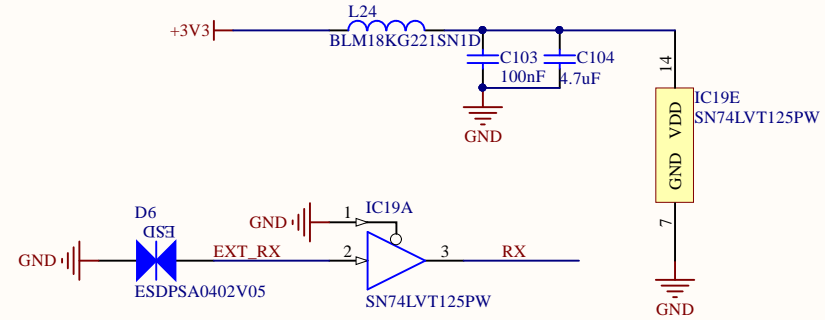
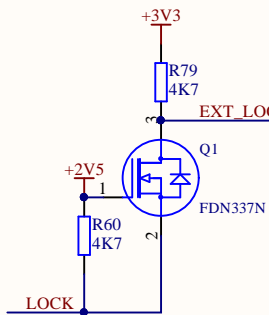
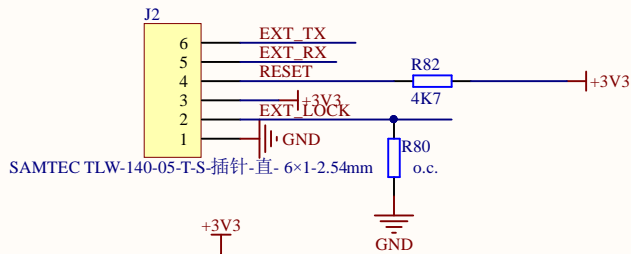


o.c.

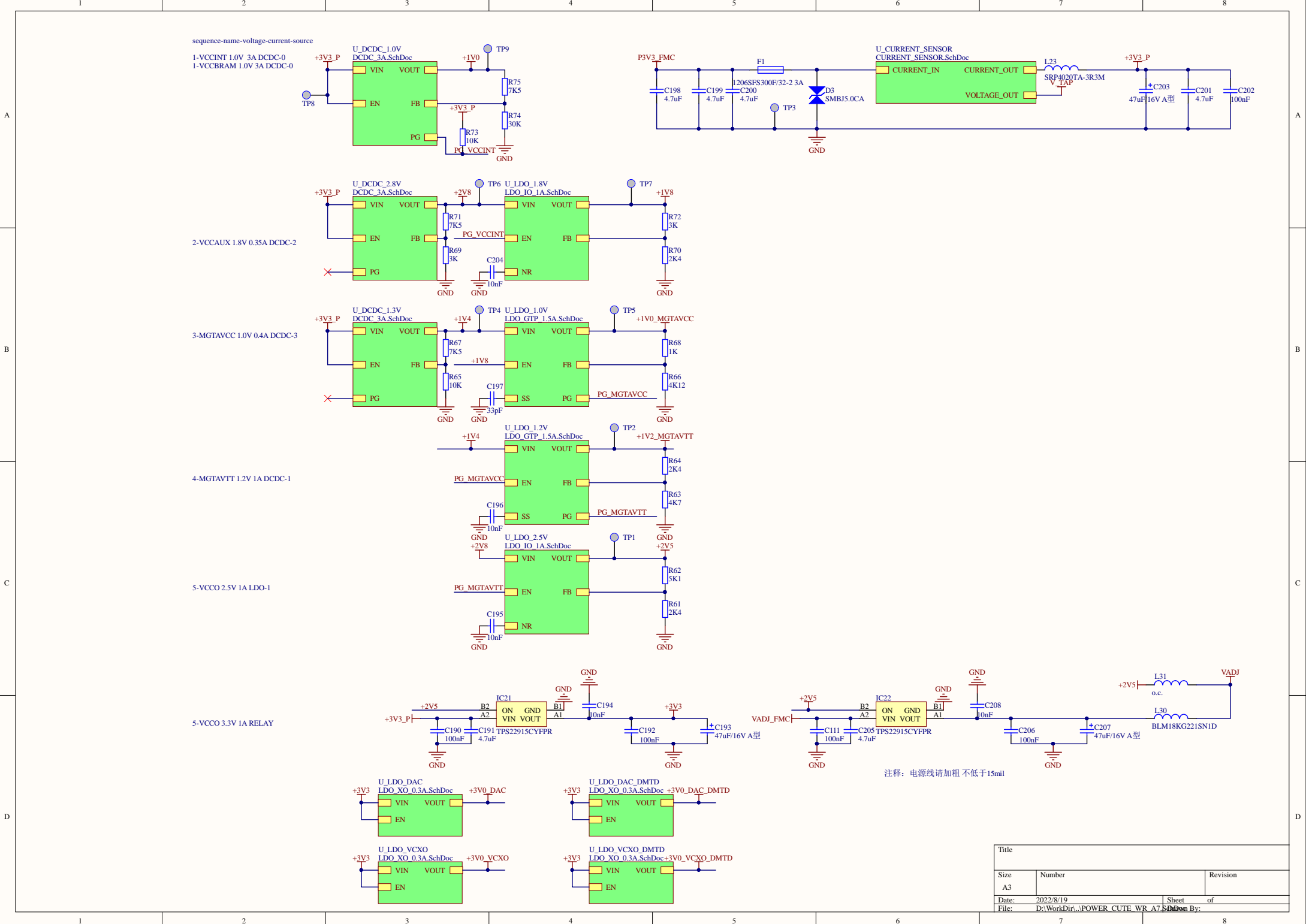
注释: LOGO与ESD可缩小



注释: 此连接器需要插拔操作, 注意留出插拔空间



Title		
Size A4	Number	Revision
Date: 2022/8/19	Sheet of	
File: D:\WorkDir\...\MISC_CUTE_WR_A7.Sch Drawn By:		



sequence-name-voltage-current-source

1-VCCINT 1.0V 3A DCDC-0
1-VCCBRAM 1.0V 3A DCDC-0

2-VCCAUX 1.8V 0.35A DCDC-2

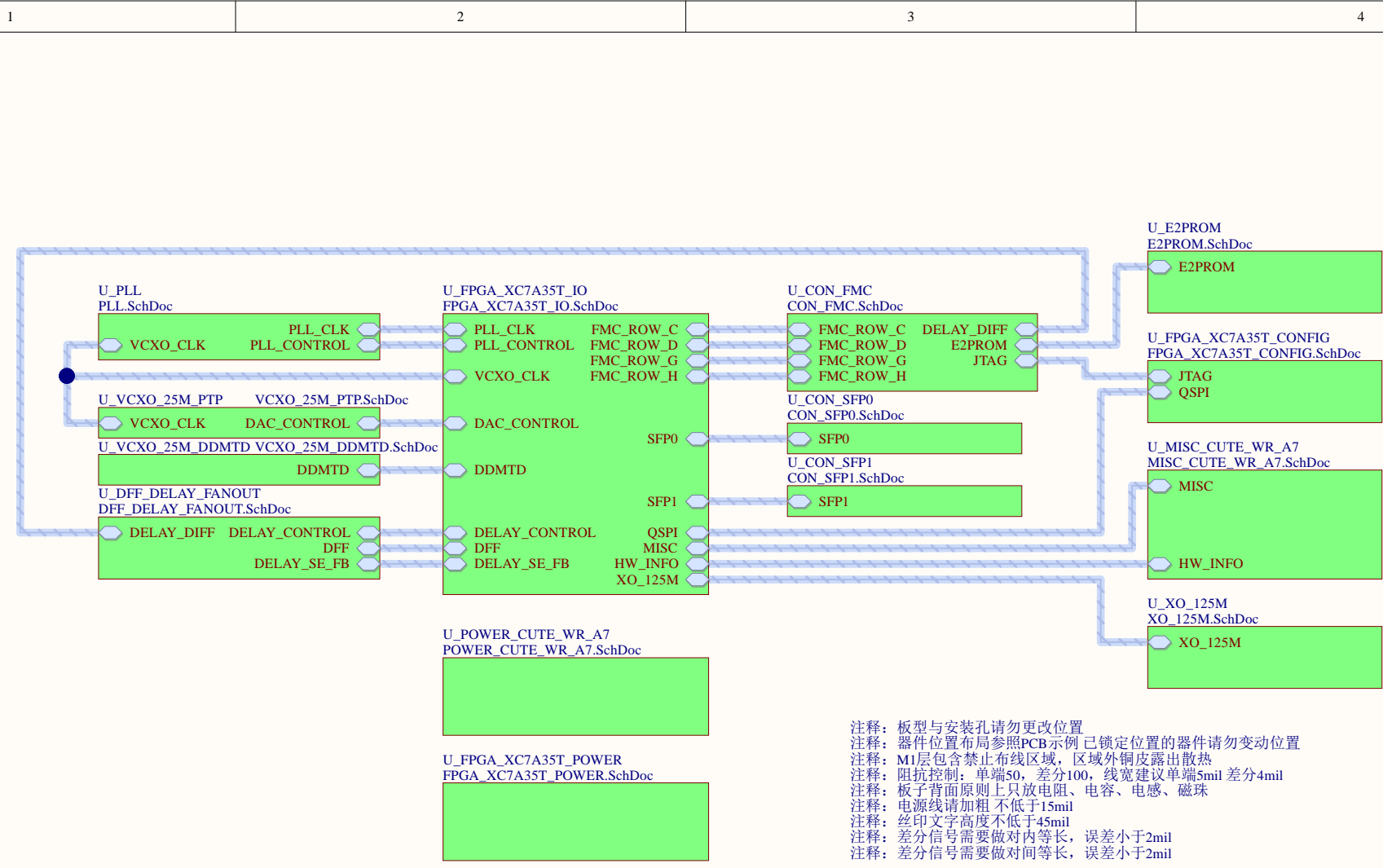
3-MGTAVCC 1.0V 0.4A DCDC-3

4-MGTAVTT 1.2V 1A DCDC-1

5-VCCO 2.5V 1A LDO-1

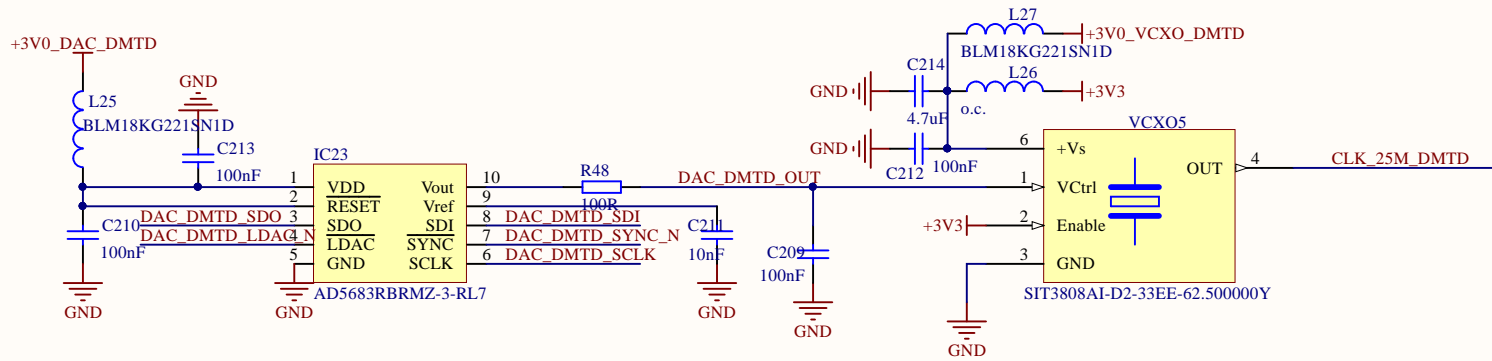
5-VCCO 3.3V 1A RELAY

Title		
Size	Number	Revision
A3		
Date:	2022/8/19	Sheet of
File:	D:\WorkDir\POWER CUTE WR_A7	Drawn By:

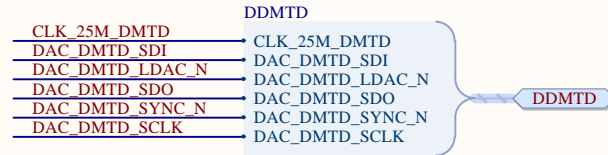


注释: 板型与安装孔请勿更改位置
 注释: 器件位置布局参照PCB示例 已锁定位置的器件请勿变动位置
 注释: M1层包含禁止布线区域, 区域外铜皮露出散热
 注释: 阻抗控制: 单端50, 差分100, 线宽建议单端5mil 差分4mil
 注释: 板子背面原则上只放电阻、电容、电感、磁珠
 注释: 电源线请加粗 不低于15mil
 注释: 丝印文字高度不低于45mil
 注释: 差分信号需要做对内等长, 误差小于2mil
 注释: 差分信号需要做对间等长, 误差小于2mil

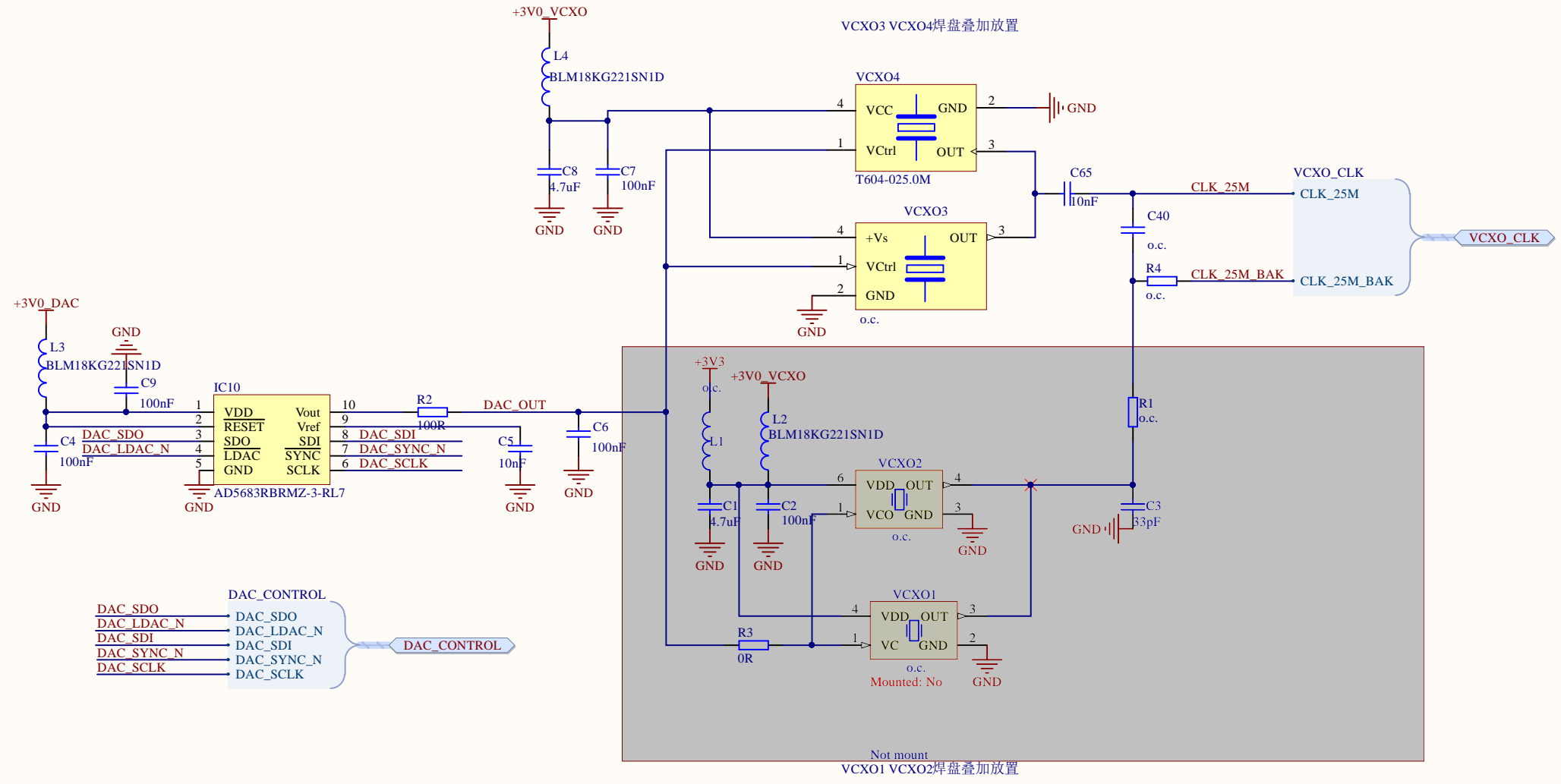
Title		
Size A4	Number	Revision
Date: 2022/8/19	Sheet of	
File: D:\WorkDir\...\TOP_CUTE_WR_A7.SchDoc	Drawn By:	



注释: DAC输出单端走线尽可能短, 地保护
 注释: CLK_25M_DMTD单端走线尽可能短, 地保护

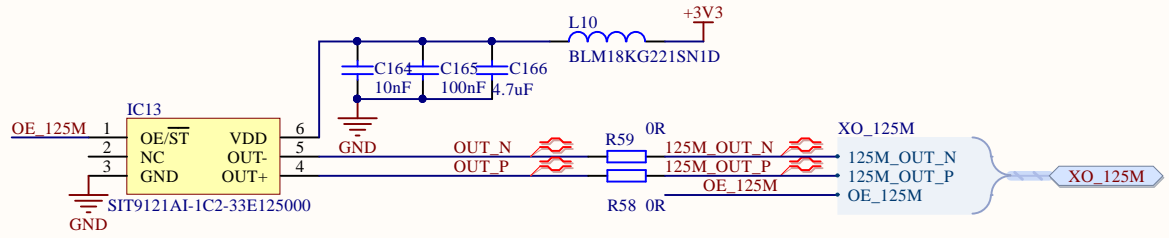


Title		
Size	Number	Revision
A4		
Date:	2022/8/19	Sheet of
File:	D:\WorkDir\...\VCXO_25M_DDMTD.Sch Drawn By:	



注释: DAC输出单端走线尽可能短, 地保护
 注释: CLK_25M CLK_25M_BAK单端走线尽可能短, 地保护

Title		
Size A4	Number	Revision
Date: 2022/8/19	Sheet of	
File: D:\WorkDir\...\VCXO_25M_PTP.SchDoc Drawn By:		



Title			
Size	Number		Revision
A4			
Date:	2022/8/19	Sheet	of
File:	D:\WorkDir\...\XO_125M.SchDoc	Drawn By:	

PCB FABRICATION NOTES

UNLESS OTHERWISE SPECIFIED, ADHERE TO LATEST NCAB GROUP PRODUCT SPECIFICATION

CONSTRUCTION
FILE SPECIFICATION
LEAD-FREE ROHS YES NO
WATERL FINISH PER NCAB STANDARD
FINAL PCB THICKNESS 0.8mm 1.0mm 1.6mm 2.0mm OTHER _____
LAYER COUNT 2 4 6 8 10 12
LAYER STACKUP SEE DETAIL DRAWING
IMPEDANCE CONTROL YES NO IF YES, SEE DETAIL DRAWING
SPECIAL CORES YES NO IF YES, SEE DETAIL DRAWING
SPECIAL TECHNOLOGY BACKDRILLING EDGE PLATING
BOARD EDGE NO METAL BURRS AND SHARP EDGES
BOW & TWIST 0.7% MAX ON PCBs WITH FINE PITCH OR BGAs
PROFILING NC-ROUTE V-SCORE BOTH AS INDICATED

CONDUCTIVE MATERIAL
CU THICKNESS INTERNAL 18um 35um 70um _____ um FINISHED
CU THICKNESS EXTERNAL 18um 35um 70um 705um FINISHED
PLATING FINISH Ni-HAL Ni-SHAL ENIG OSP
 NiAg NiSn OTHER _____

SELECTIVE Au PLATING NO YES ON EDGE FINGERS AS INDICATED
INTERCONNECTS
DRILL PROCESS TH BLIND / BURIED LASER MICROVIA
HOLE WALL PLATING 25um NOMINAL
AS SPECIFIED IN TABLE, AFTER THROUGH PLATING
HOLE SIZE 0.10 0.15 0.2 0.25 LARGER
VIA HOLE PLUGGING NO YES, WITH FILL >70%
PLATING OVER PLUGGING YES NO
PLUGGING TYPE RESIN COPPER SOLDERMASK

COSMETICS
SOLDERMASK SIDES TOP BOT BOTH SIDES
SOLDER MASK TYPE PHOTO IMAGEABLE MATT GLOSS
SOLDER MASK COLOUR GRN BLUE RED WHITE BLACK
SOLDER MASK MATERIAL MUST COMPLY TO IPC-8M40 CLASS-T
SOLDER MASK THICKNESS SURFACE BETWEEN 10um and 30um; 25um ON KNEE

SILKSCREEN COLOUR WHITE BLACK OTHER _____
SILKSCREEN PRINT NON-CONDUCTIVE INK
SILKSCREEN QTY TOP BOT BOTH SIDES NONE
SILKSCREEN LINE WIDTH 0.175mm 0.2mm
SILKSCREEN OVER PADS NOT PERMITTED, TRIM IF OVER PADS

MANUFACTURING DEVIATIONS
PAD REMOVAL ONLY ALLOWED ON UNUSED PADS ON INNER LAYERS
TEARDROPPING FOLLOW GERBER, RAISE EQ IF REQUIRED
THROWING ON PANEL STRIPS ONLY, EQ IF NEEDED ELSEWHERE.
VIA SIZE REDUCTION RAISE EQ IF REQUIRED

ADDITIONAL REQUIREMENTS
ELECTRICAL TEST ALWAYS
DATE CODE ALWAYS
FACTORY LOGO YES NO
UL LOGO YES NO

CLEANLINESS PER NCAB GROUP SPECIFICATION
CROSS-SECTION PER SEC. 10 SEC. THERMAL SHOCK 3 TIMES
PEELABLE BLUE TYPE PRETERS 2955
X-OUTS ON PANEL NO
HAL PLATING THICKNESS >10um
ENIG PLATING THICKNESS BETWEEN 0.05um and 0.125um

NCAB TEST REPORT YES

SPECIAL INSTRUCTIONS

- 1)
- 2)
- 3)
- 4)
- 5)

CAD CONFIGURATION BY: EDA TECHNOLOGIES

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Over Lay				
2	Top Solder	Solder Resist	0.10mil	3.5	
3	Top	Copper	1.20mil		
4	Dielectric 1	FR-4	3.91mil	4.2	
5	SDP2	Copper	0.60mil		
6	Dielectric 2	FR-4	3.91mil	4.2	
7	RTD9	Copper	0.60mil		
8	Dielectric 3	FR-4	9.00mil	4.2	
9	RTD1	Copper	0.60mil		
10	Dielectric 4	FR-4	3.91mil	4.2	
11	SDP5	Copper	0.60mil		
12	Dielectric 11	FR-4	3.91mil	4.2	
13	SDP6	Copper	1.20mil		
14	Dielectric 14	FR-4	3.91mil	4.2	
15	SDP7	Copper	1.20mil		
16	Dielectric 5	FR-4	3.91mil	4.2	
17	SDP8	Copper	0.60mil		
18	Dielectric 16	FR-4	3.91mil	4.2	
19	RTD10	Copper	0.60mil		
20	Dielectric 17	FR-4	3.91mil	4.2	
21	RTD10	Copper	0.60mil		
22	Dielectric 18	FR-4	3.91mil	4.2	
23	SDP11	Copper	0.60mil		
24	Dielectric 19	FR-4	3.91mil	4.2	
25	Bottom	Copper	1.20mil		
26	Bottom Solder	Solder Resist	0.10mil	3.5	
27	Bottom Over Lay				

SINGLE TRACE IMPEDANCE CONTROL

LAYER	WIDTH (mil)	IMPEDANCE (ohm)	PRECISION	FREQUENCY (MHz)	REMARK
TOPBOT	5.1	50	±10%	DEFAULT	
RTD9,04,09,10	4.6	50	±10%	DEFAULT	
			±10%	DEFAULT	
			±10%	DEFAULT	

If impedance line without ref layers or with incomplete ref layers, need issue EQ confirm.

DIFFERENTIAL PAIR IMPEDANCE CONTROL

LAYER	WIDTH-SPACE (mil)	IMPEDANCE (ohm)	PRECISION	FREQUENCY (MHz)	REMARK
TOPBOT	4.1-7.5	100	±10%	DEFAULT	
RTD9,04,09,10	4-7.6	100	±10%	DEFAULT	
			±10%	DEFAULT	
			±10%	DEFAULT	

If impedance line without ref layers or with incomplete ref layers, need issue EQ confirm.

DATE:	2020/06/23
DRAWN BY:	NCAB
ENGINEER:	Jing-Chai



PCB NAME:	CD12375	SCALE:	1:1
DOC NUMBER:	CD12375	SHEET:	1 of 1
PROJECT FILENAME:	CD12375	PCB FILENAME:	CD12375
		REVISION:	1

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